REMARKS

In response to the Office Action mailed July 7, 2005, Applicants respectfully request reconsideration. Claims 1-12 were previously pending in this application. Claim 1 has been amended. New claims 13-32 have been added to more fully define Applicants' contribution to the art. As a result, claims 1-32 are pending for examination with claims 1 and 13 being independent claims. No new matter has been added.

Rejections Under 35 U.S.C. §103

The Office Action rejected claims 1-12 under 35 U.S.C. §103(a) as being unpatentable over Pasotti et al., (U.S. Patent No. 6,535,428) in view of Conte et al. (U.S. Patent No. 6,320,808). Applicants respectfully traverse this rejection.

Applicants do not agree that there exists motivation to combine the Conte et al. and Pasotti et al. references. However, the motivation to combine the references will not be discussed further herein. Applicants reserve the right to raise this issue at a later date.

Conte et al. is directed to a memory read amplifier circuit including a differential comparator circuit (Abstract). FIG. 1 illustrates that the memory read amplifier includes two branches. The branches include two PMOS transistors coupled in a current mirror configuration.

Pasotti et al. is directed to a sensing circuit that includes two branches (Abstract). The first branch includes a MOSFET MP1 and a transistor MN1 coupled to a memory cell MC1. The second branch includes a MOSFET MP2 and a transistor MN2 coupled to a reference memory cell RC1.

MOSFETs MN1 and MN2 are used to bias the drain electrode of the memory cell MC1 and the reference cell RC1, respectively (col. 5, lines 10-12). FIG. 3 shows a bias voltage generator 13 that biases gate electrodes of MOSFETs MN1 and MN2. As illustrated in FIG. 3, bias voltage generator 13 includes an operational amplifier OP1 having an output coupled to transistor MN1 and an inverting input coupled to the drain of memory cell MC1.

MOSFETs MP1 and MP2 form a current mirror and a bi-stable latch structure (col. 4, lines 31-34). "MOSFETs MP1 and MP2 behave as current-voltage converters, converting respective currents IC and IR flowing therethrough into voltage signals at nodes N1 and N2, respectively" (col. 5, lines 45-47). As shown in FIG. 1, MOSFETs MP1 and MP2 are connected

to respective inputs of a comparator 14, which compares signals at nodes N1 and N2 (col. 5, lines 53-54).

By contrast, claim 1, as amended, recites, *inter alia*, a first load for connection between a supply terminal and an input terminal of an output comparator, said first load being connected to said reference cell, and a second load, connectable to a nonvolatile memory cell, said first load and said second load each having a controllable resistance, and a control circuit controlling said first load and said second load and feeding said first load and said second load with a control voltage independent of an operating voltage between a first conduction terminal and a second conduction terminal of said first load. Neither Pasotti et al. nor Conte et al. teach or suggest a first load for connection between a supply terminal and an input terminal of an output comparator and a control circuit controlling the first load and feeding the first load with a control voltage independent of an operating voltage between a first conduction terminal and a second conduction terminal of the first load. Therefore, claim 1 patentably distinguishes over Pasotti et al. and Conte et al. either alone or in combination. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 2-12 depend from claim 1 and are therefore patentable for at least the same reasons.

New Claims

New claim 13 relates to a sense amplifier that includes a reference memory cell and a first transistor. The first transistor has a first conducting terminal coupled to the reference memory cell and a second conducting terminal for connection to a supply voltage. Sense amplifier further includes a control circuit coupled to a control input of the first transistor and a first conducting terminal of the first transistor such that the control circuit applies a control voltage to the control input that is substantially independent of a voltage difference between a voltage of the first conducting terminal and the supply voltage. Claim 13 is patentable over Pasotti et al. and Conte et al. because neither Pasotti et al. nor Conte et al. teach or suggest a first transistor having a first conducting terminal coupled to the reference memory cell and a second conducting terminal for connection to a supply voltage and a control circuit coupled to a control input of the first transistor.

Claims 14-32 depend from claim 13 and are therefore patentable for at least the same reasons.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
Marco PASOTTI et al., Applicants

By: _____

James H. Morris, Reg. No. 34,681
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
Telephone: (617) 646-8000

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